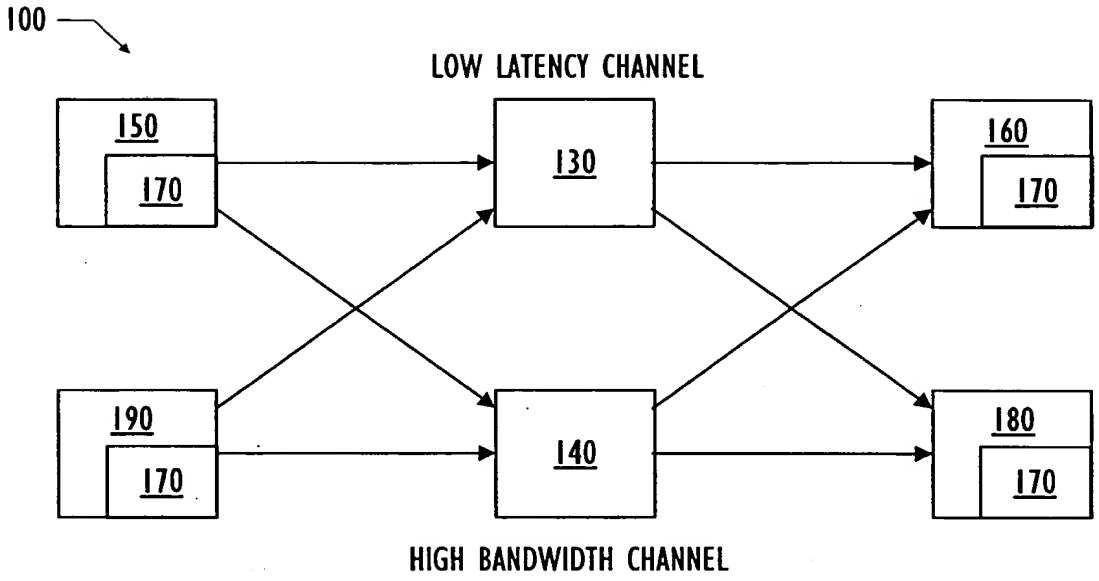


FIG. 1

09/470,760 12/23/1999

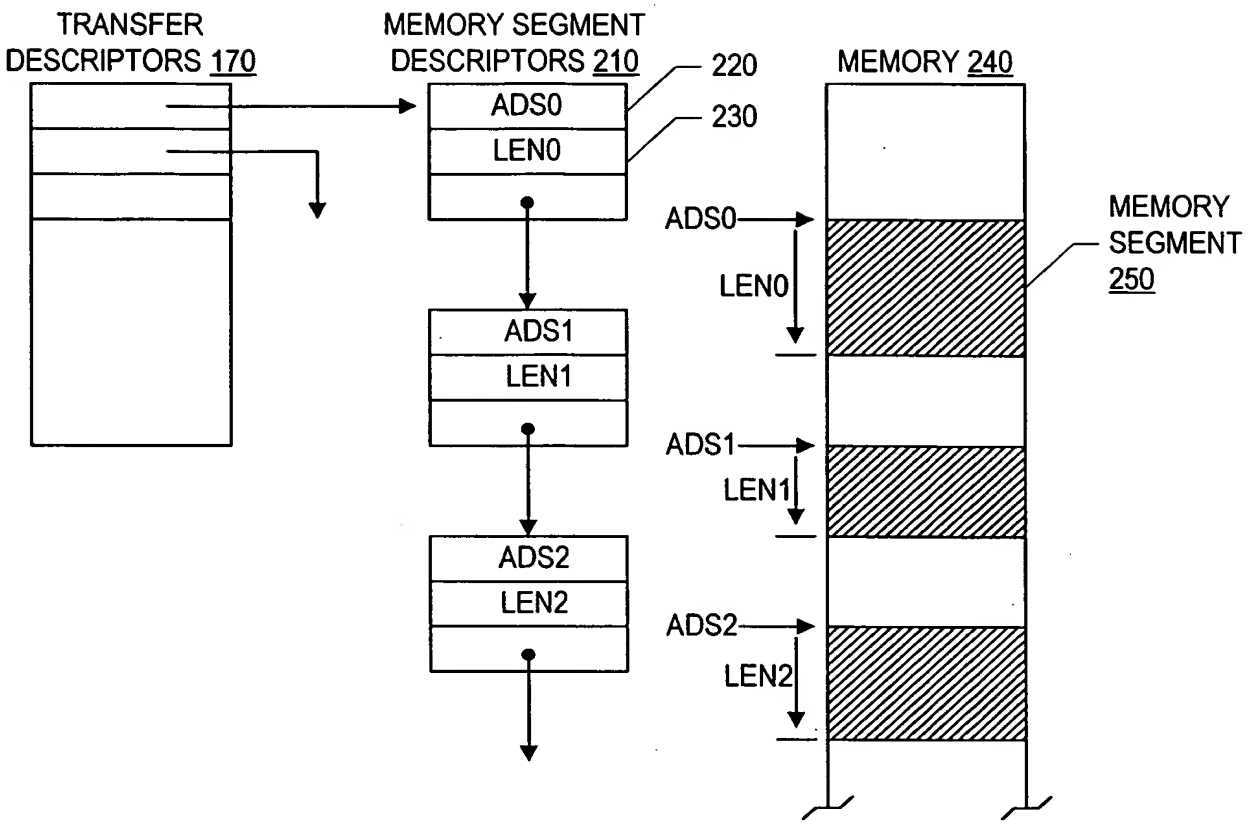

TRANSFER
DESCRIPTORS 170
MEMORY SEGMENT
DESCRIPTORS 210
220
230
MEMORY 240
ADS0
LEN0
ADS1
LEN1
ADS2
LEN2
ADS0
LEN0
ADS1
LEN1
ADS2
LEN2
MEMORY
SEGMENT
250

FIG. 2

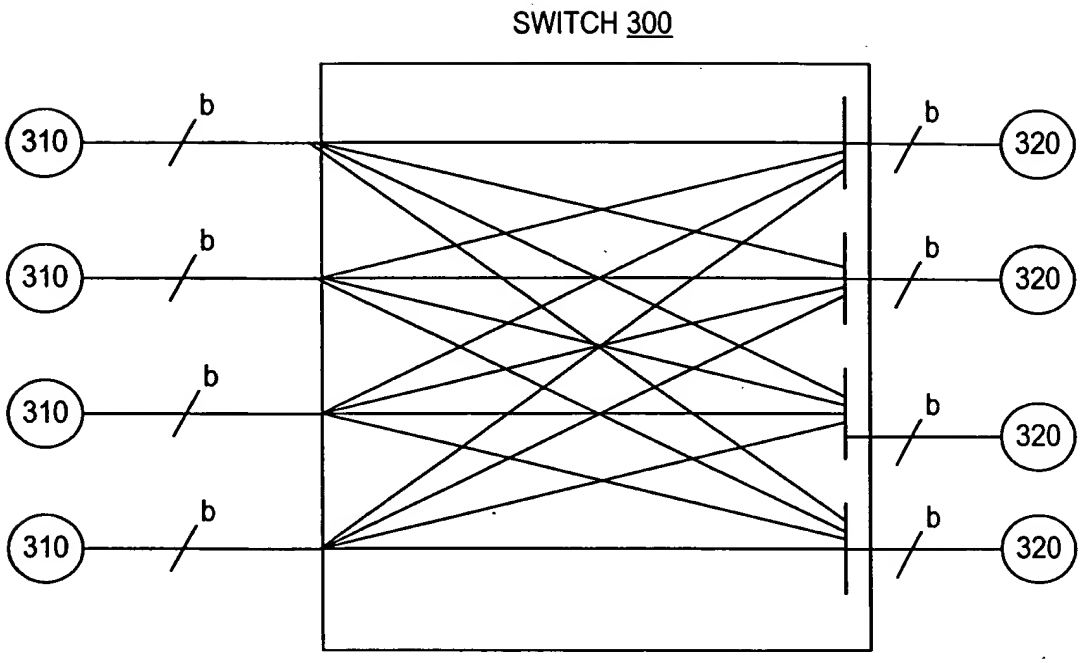


FIG. 3

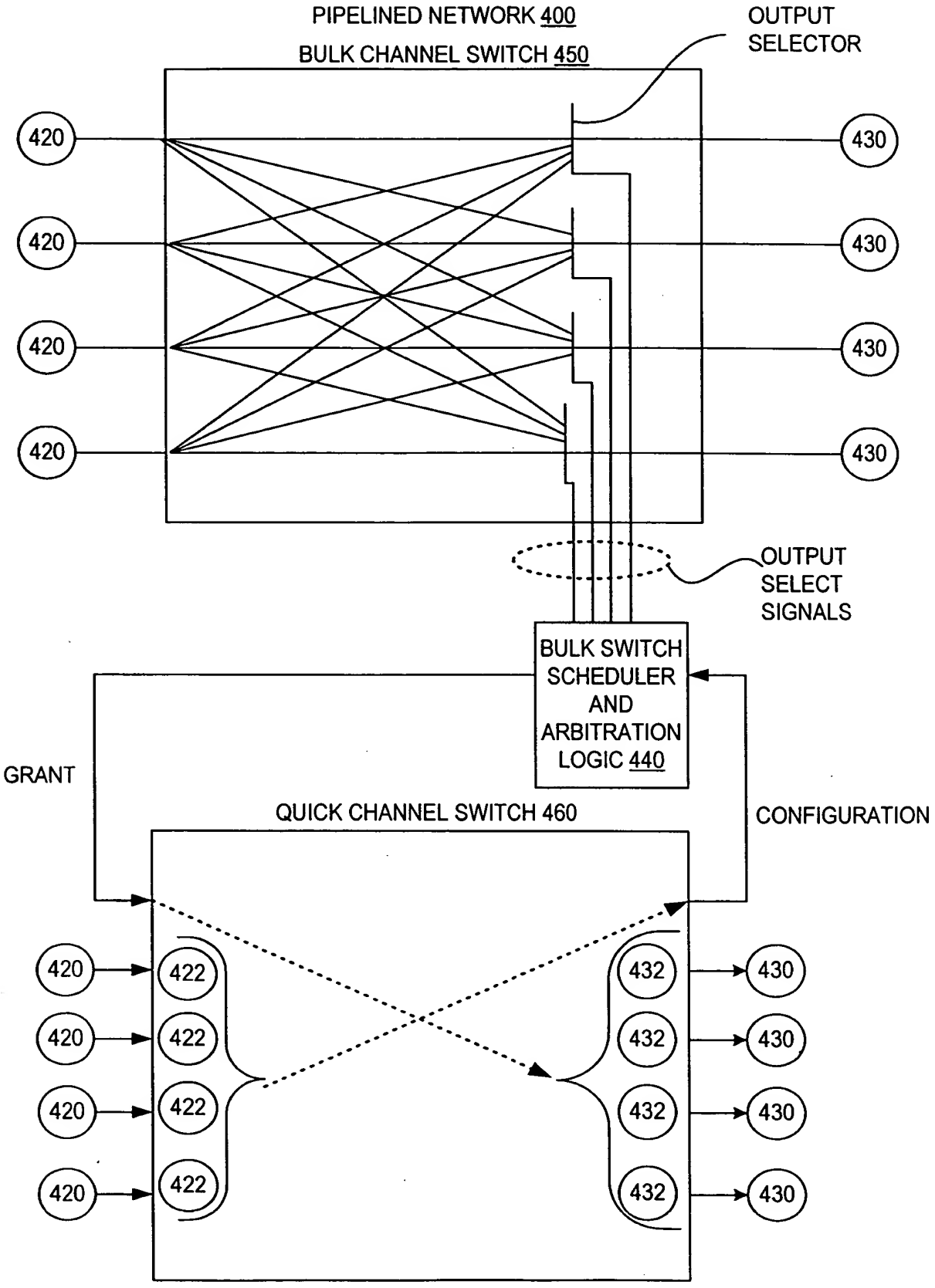


FIG. 4

DOCKET: 6540.0050

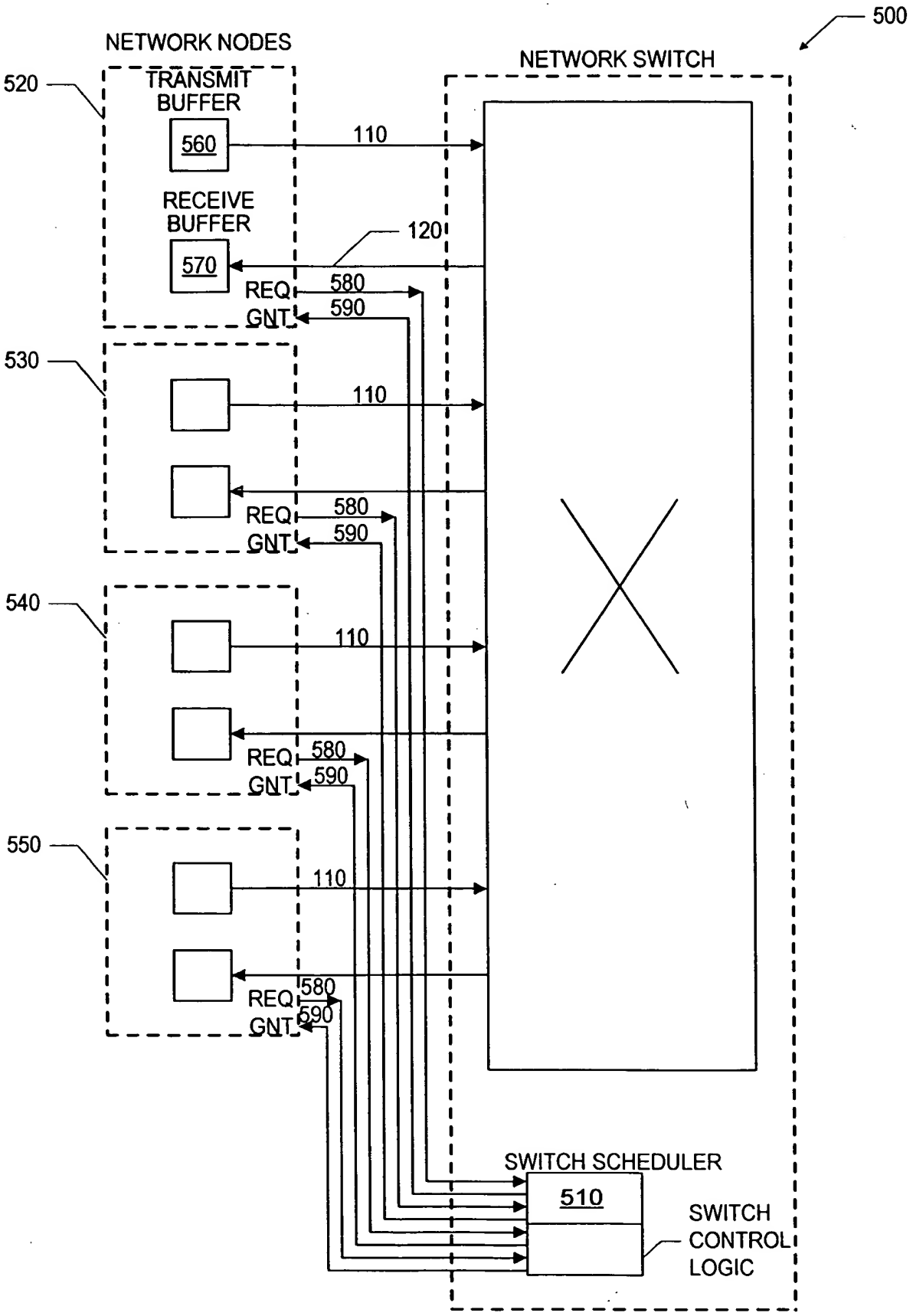

500
NETWORK NODES
NETWORK SWITCH
520
TRANSMIT BUFFER
560
110
RECEIVE BUFFER
570
120
REQ
GNT
580
590
530
540
550
SWITCH SCHEDULER
510
SWITCH CONTROL LOGIC

FIG. 5

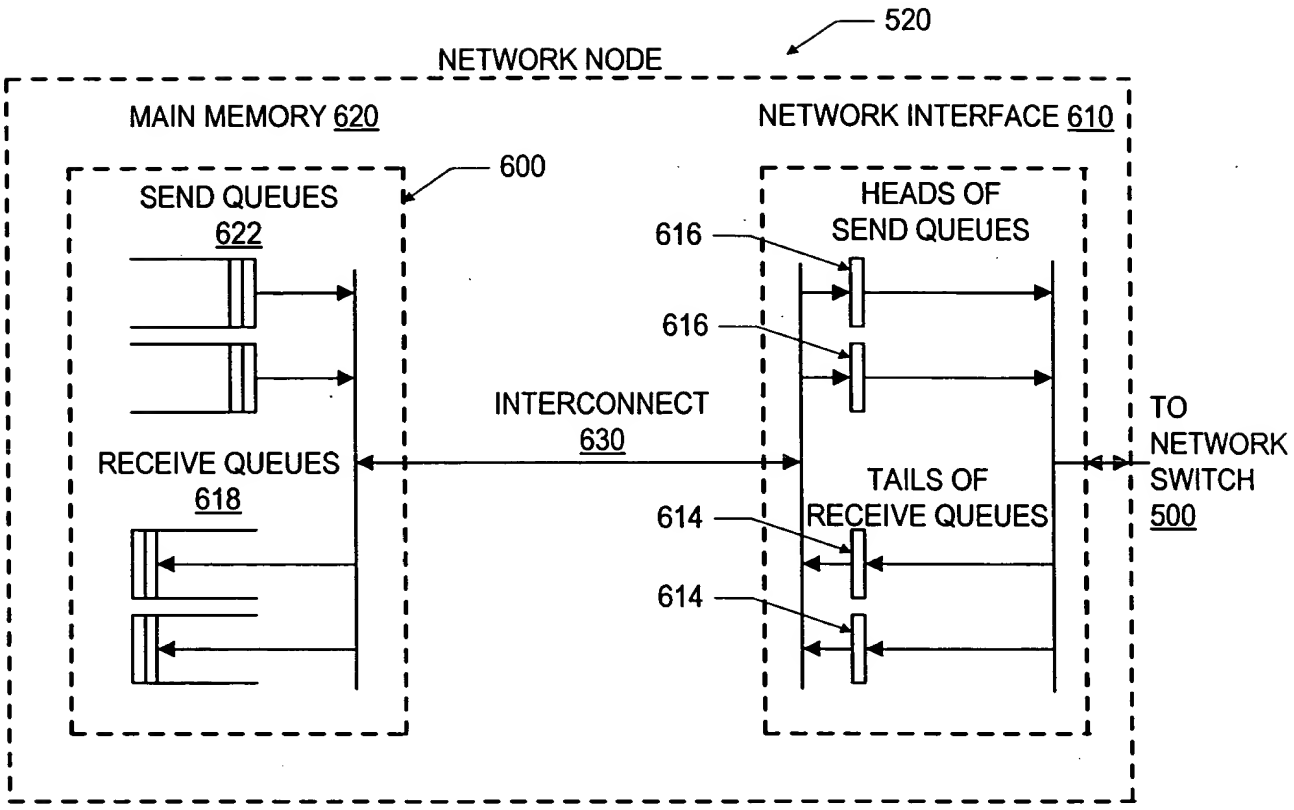


FIG. 6

0015-6750-0403-0950-7

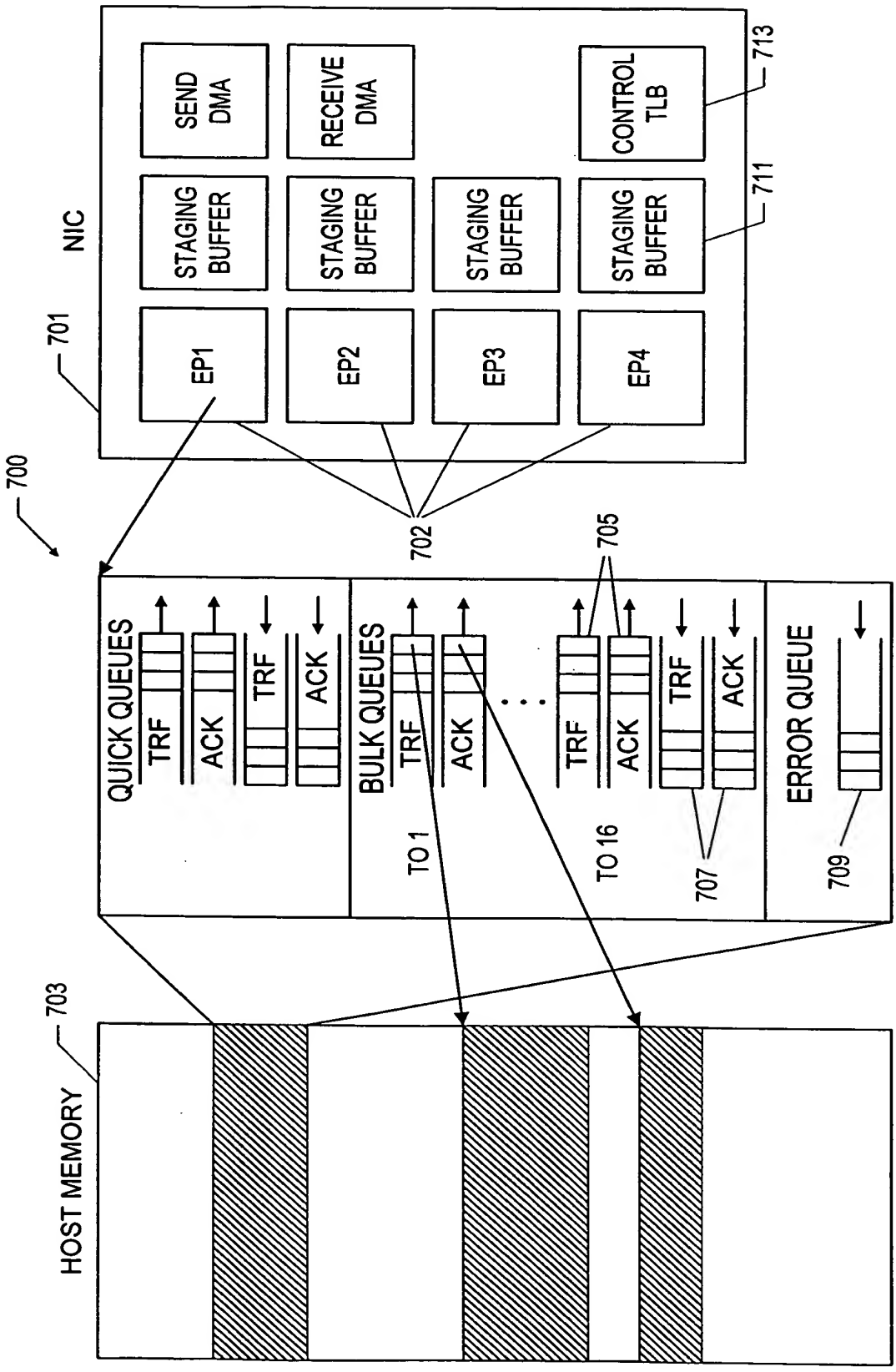

700
NIC
701
EP1
EP2
EP3
EP4
STAGING BUFFER
STAGING BUFFER
STAGING BUFFER
STAGING BUFFER
711
SEND DMA
RECEIVE DMA
CONTROL TLB
713
702
705
QUICK QUEUES
TRF
ACK
TRF
ACK
BULK QUEUES
TRF
ACK
TO 1
TRF
ACK
TRF
ACK
TO 16
707
ERROR QUEUE
709
HOST MEMORY
703

FIG. 7

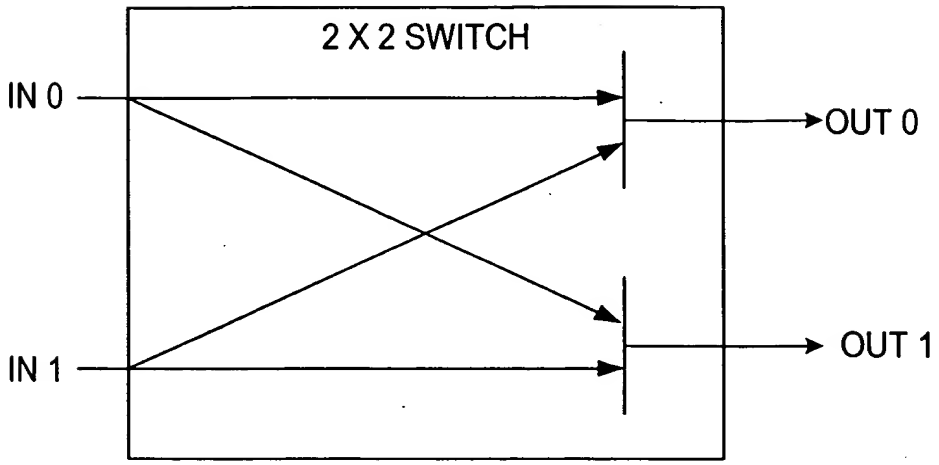


FIG. 8

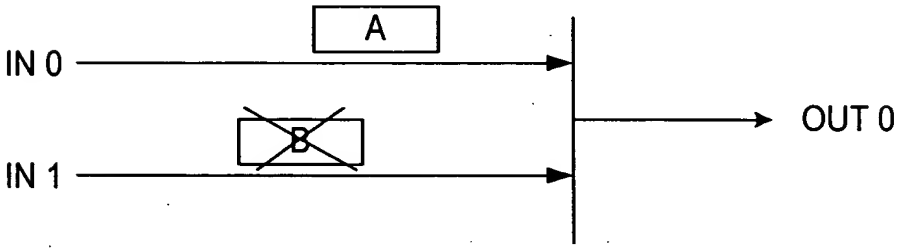


FIG. 9A

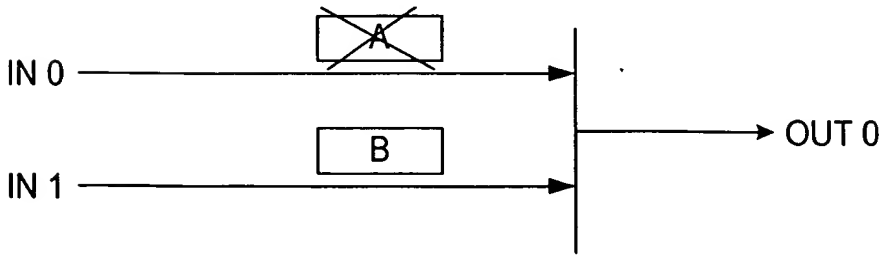


FIG. 9B

DOCID: 02704959

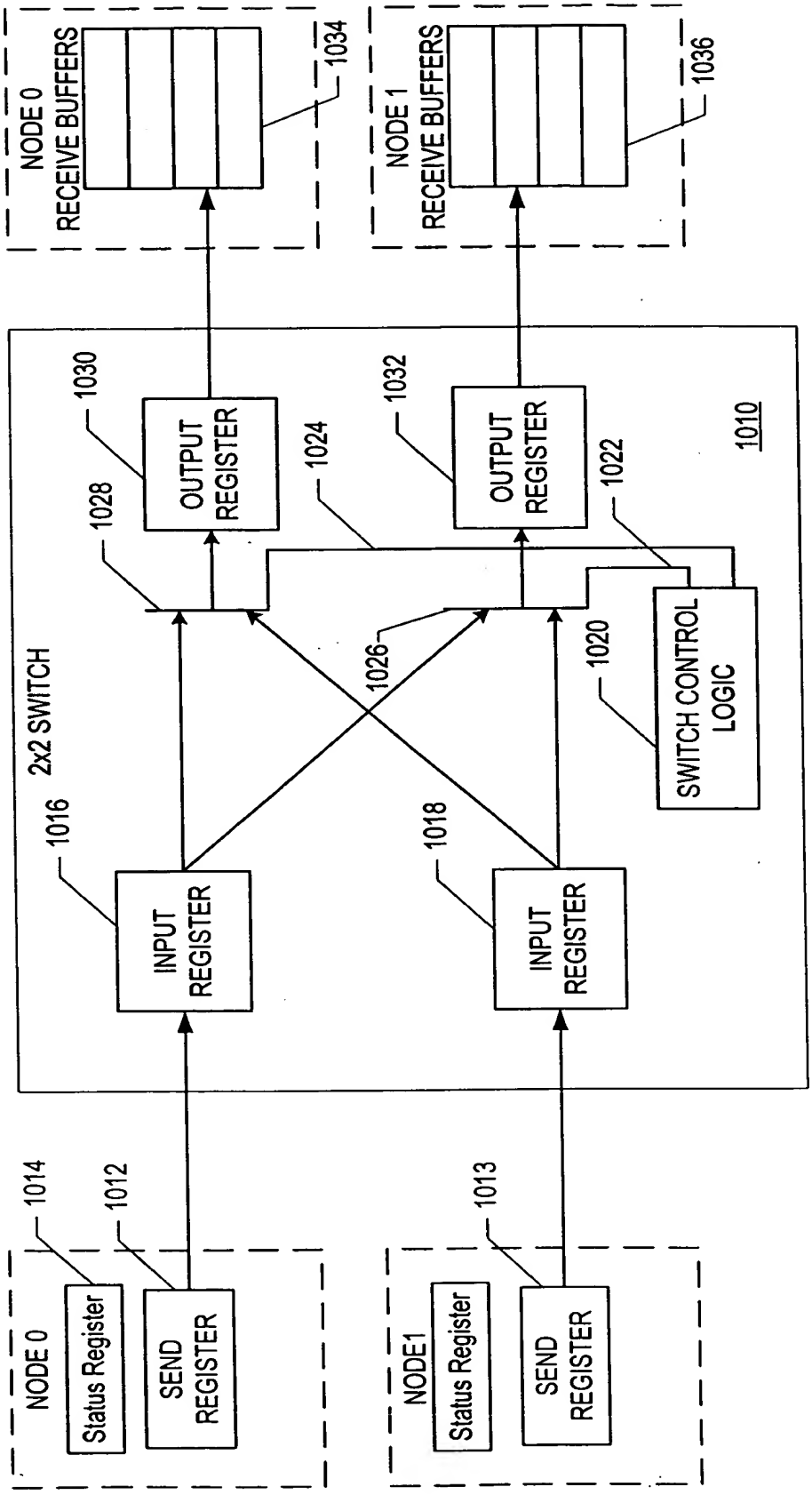

NODE 0
RECEIVE BUFFERS
1034
NODE 1
RECEIVE BUFFERS
1036
1030
OUTPUT REGISTER
1032
OUTPUT REGISTER
1028
1024
1022
1010
2x2 SWITCH
1026
1020
SWITCH CONTROL LOGIC
1016
INPUT REGISTER
1018
INPUT REGISTER
1014
1012
1013
NODE 0
Status Register
SEND REGISTER
NODE1
Status Register
SEND REGISTER

FIG. 10

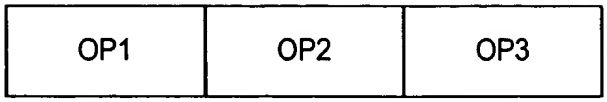


FIG. 11A

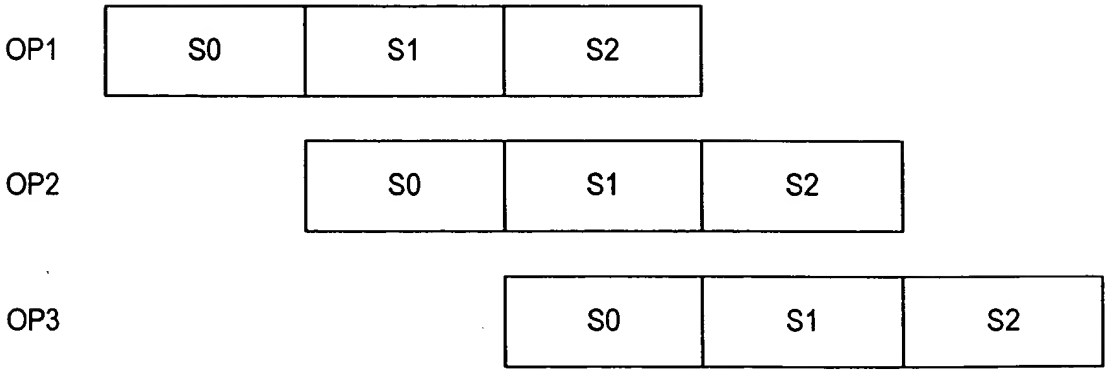


FIG. 11B

Docket No. 50277-2000

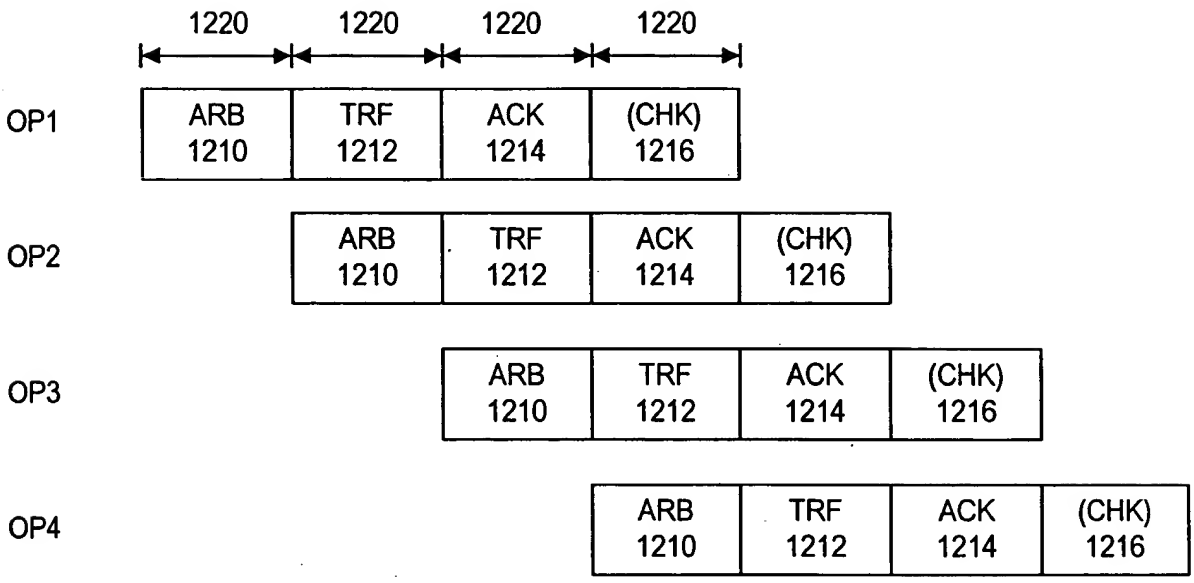
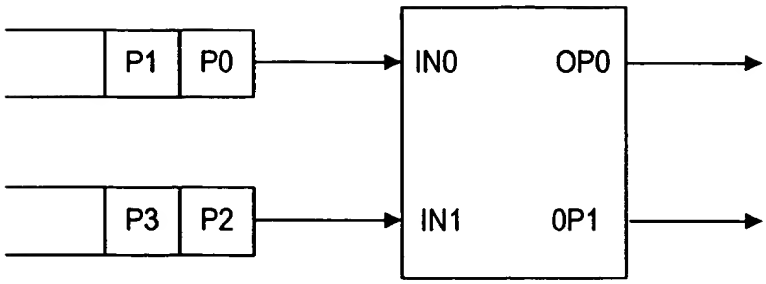


FIG. 12

0054026-0030100



PACKETS P0, P2 ARE DESTINED FOR O0
PACKETS P1, P3, ARE DESTINED FOR O1

FIG. 13

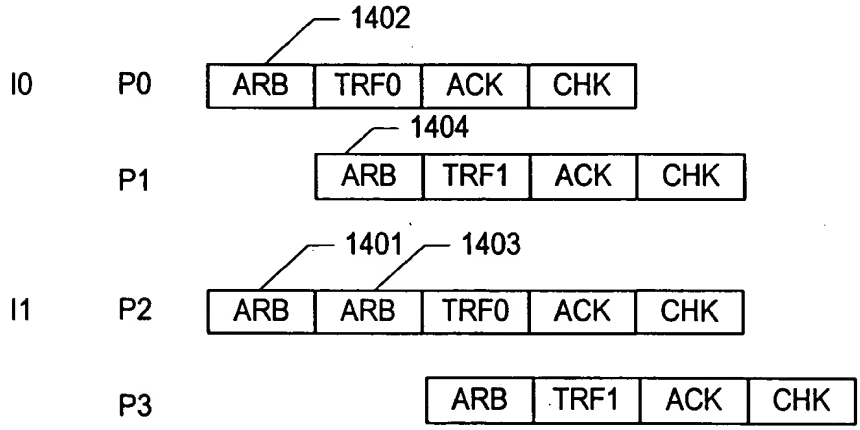


FIG. 14

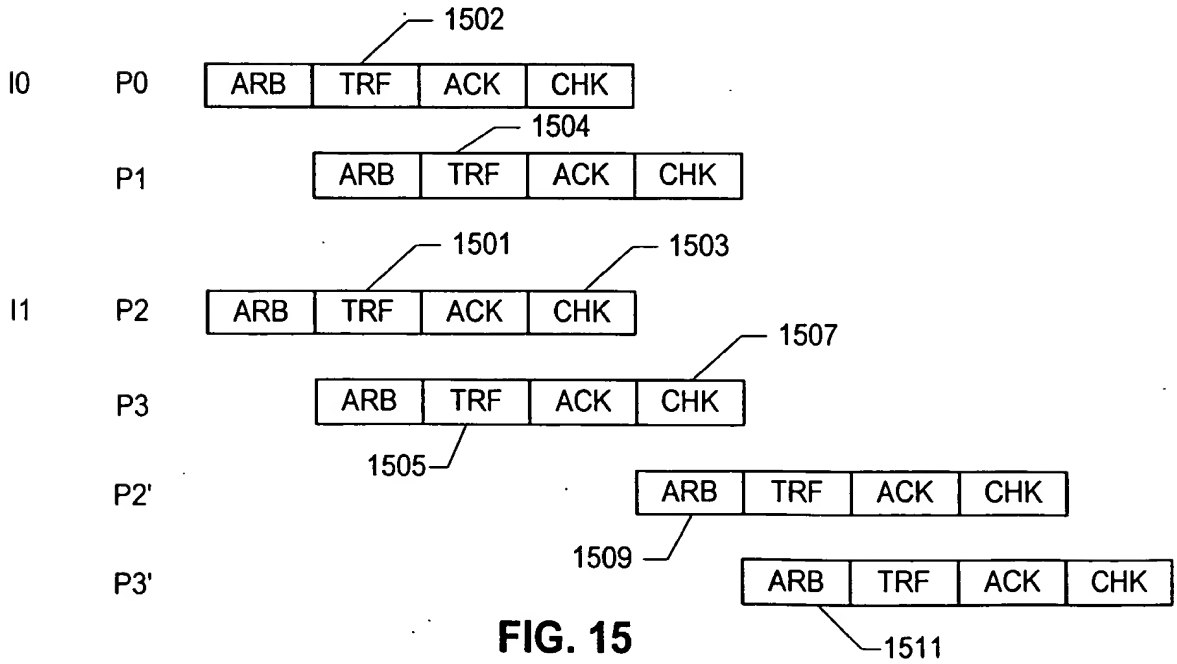


FIG. 15

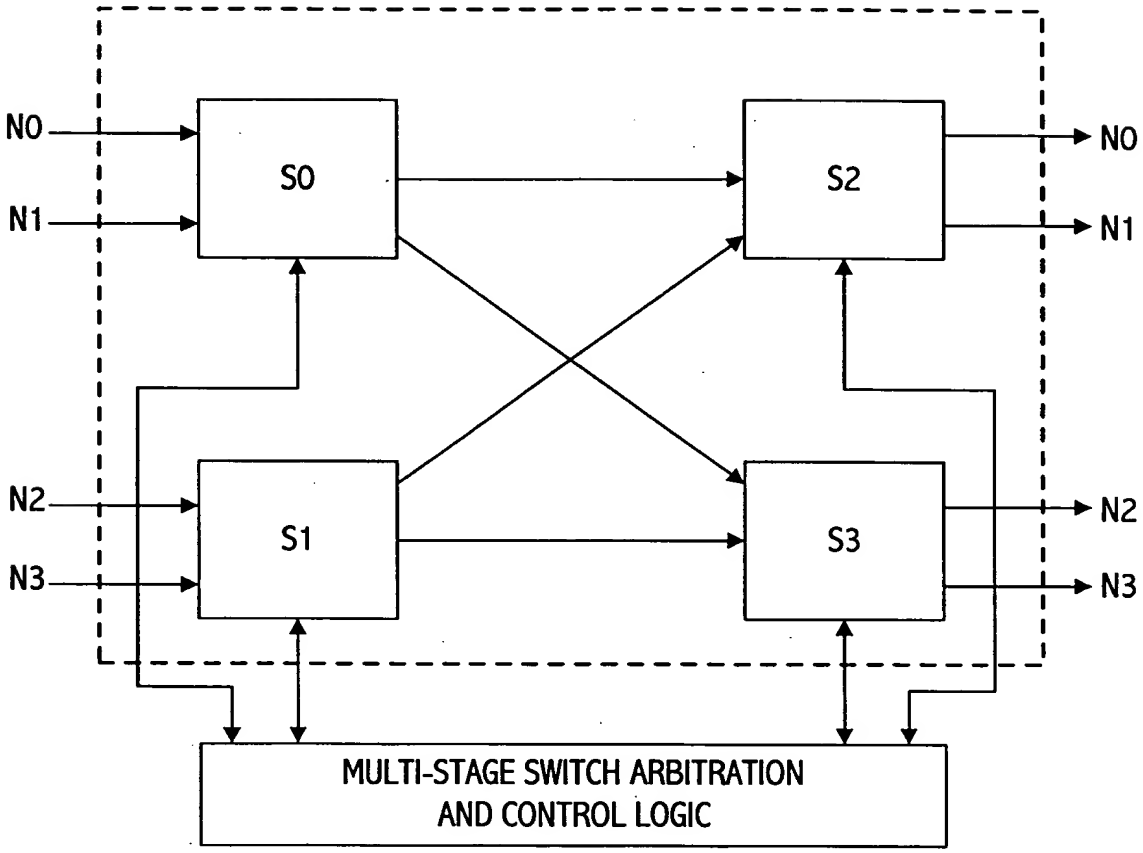


FIG. 16

09540760 - 030100